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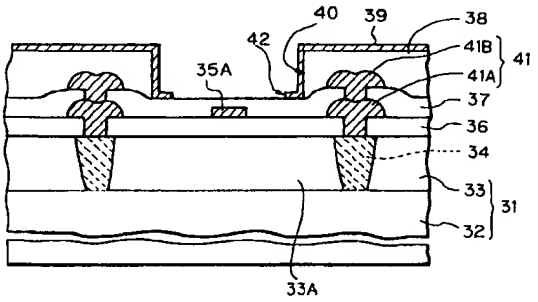
(54) Semiconductor device with fuse.

(57) A semiconductor device with a fuse comprises: a semiconductor substrate (31); a field oxide layer (36); a fuse (35) formed on the field oxide layer (36); an insulating layer (37) over the fuse (35) and the field oxide layer (36); a passivation layer (38) formed on the insulating layer (37) and having an opening above the fuse (35); and a nitride layer (39) formed on the passivation layer (38). It also comprises a metal guard ring (41) which surrounds a narrow blowable portion (35A) of the fuse (35), and is formed under the passivation layer (38) to extend to the semiconductor substrate (31) through the insulating layer (37) and the field oxide layer (36). The semiconductor substrate (31) consists of a base semiconductor substrate (32) and an epitaxial semiconductor layer (33) and is provided with an isolation region (34) which region is formed in the epitaxial semiconductor layer (33) so as to completely surround and isolate a portion (33A) of the epitaxial layer below the narrow portion (35A), and the metal guard (41) that comes into direct contact with the isolation region (34).

Fig. 3B



EP 0 531 128 A1

The present invention relates to a semiconductor device (e.g., memory device) including fuses used for redundant circuitry programming. For example, fuses are formed in a decoder of a static random-access memory (SRAM).

A fuse of the semiconductor device is blown as needed using an electric current pulse or laser for replacing a defective circuit with a redundant circuit or for programming (writing) information in a memory cell. A partial structure of the semiconductor device including a fuse has been designed to prevent an electric short-circuit between a semiconductor substrate and a circuit including the fuse from occurring and to prevent moisture from entering into an interior of the device from the atmosphere.

Two conventional semiconductor devices with a fuse are now explained with reference to Figs. 1A, 1B, 2A and 2B, respectively.

As shown in Figs. 1A and 1B, a portion of a first conventional semiconductor device including a fuse comprises a semiconductor substrate 1 consisting of a p-type silicon base substrate 2 and an n-type epitaxial silicon layer 3 formed thereon. In the epitaxial layer 3 a p-type isolation region 4 of a rectangular ring (Fig. 1A) is formed to extend in the base substrate 2, so that a portion 3A of the epitaxial layer below a narrow blowable portion 5A of a fuse 5 is isolated from the base substrate 2 and the other portion of the epitaxial layer 3. On the substrate 1 (i.e., the epitaxial layer 3) a field oxide layer 6 of SiO_2 is formed. The fuse 5 of polycrystalline silicon, aluminum or another metal is formed on the field oxide layer 6 and has the narrow portion 5A (Fig. 1A) to be blown. An insulating layer 7 of, e.g., PSG (phosphosilicate glass) is formed over the fuse 5 and the field oxide layer 6 for isolating lower interconnections (conductive lines) including the fuse from upper interconnections. Furthermore, a passivation layer 8 of, e.g., PSG is formed on the insulating layer 7, and a nitride layer 9 of, e.g., Si_3N_4 is formed on the passivation layer 8. Since the passivation PSG layer 8 has hygroscopicity (i.e., low moisture-resistance), the nitride layer 9 having a high moisture-resistance prevents moisture from penetrating into the semiconductor device. The layers 9 and 8 are selectively etched to form and opening 10 above the narrow portion 5A.

As the occasion demands, the narrow portion 5A of the fuse 5 is irradiated with a laser beam through the opening 10, or a pulse current is fed through the fuse 5, so as to blow the fuse 5 by breaking the narrow portion 5A. The opening 10 facilitates the breaking of the narrow portion, and the insulating layer 7 prevents the broken portion from splashing.

When fusing, the broken portion of the fuse 5 may cause damage (cracks) to the field oxide layer 6 to extend into the epitaxial layer 3, so that there is a short circuit between the fuse 5 and the epitaxial layer 3 causing trouble. The isolation region 4 is formed to prevent the short from causing trouble.

As shown in Figs. 2A and 2B, a portion of a second conventional semiconductor device including a fuse comprises a semiconductor substrate 11 and a field oxide layer 16 of SiO_2 formed on the substrate. The substrate 11 may consist of a silicon base substrate and an epitaxial layer formed thereon. A fuse 15 with a narrow blowable portion 15A is made of polycrystalline silicon, aluminum or another metal is formed on the field oxide layer 16. An insulating layer of, e.g., PSG is formed over the fuse 15 and the field oxide layer 16 for isolating lower interconnections (conductive lines) including the fuse from upper interconnections. The insulating layer 17 is selectively etched to form a groove surrounding the narrow portion 15A except for two portions corresponding to the fuse 15. A metal guard ring 21 of, e.g., aluminum is formed to overfill the groove and come into contact with the field oxide layer 16. The guard ring 21 is separated into two portions with a light channel shape, as shown in Fig. 2A.

As mentioned in the first conventional device, a passivation layer 18 of, e.g., PSG is formed over the metal guard ring 21 and the insulating layer 17, and a nitride layer 19 of, e.g., Si_3N_4 is formed on the passivation layer 18. The layers 19 and 18 are selectively etched to form an opening 20 above the narrow portion 15A. The fuse 15 is blown by breaking the narrow portion 15A with a laser beam or a pulse current. Of course, some of a number of the fuses are selectively blown in accordance with demands, while the majority of the fuses are not blown.

Since portions of the insulating 17 and the passivation layer 18 are exposed in the opening 20, moisture penetrates into the inside of the device through the layers 17 and 18. To prevent the moisture penetration, the metal guard ring 21 is formed to vertically extend through the insulating layer 17 and to separate a portion of the layer 17 near the narrow portion 15A from the rest thereof.

However, in the first conventional semiconductor device (Figs. 1A and 1B), the moisture penetrates into the inside of the device through the insulating layer 7 and an interface between the layers 7 and 8 from the exposed portion thereof in the opening 10. The moisture in the inside deteriorates aluminum interconnections (lines) and active elements (e.g., transistors) of the device. Furthermore, when the cracks of the insulating layer 6 and the passivation layer 7 are caused by blowing the fuse 5, moisture may penetrate through interfaces between the layers 6 and 7 and between the epitaxial layer 3 and the layer 6 from the cracks. In the second conventional semiconductor device (Figs. 2A and 2B), when blowing the fuse 15, cracks in the layers 16 and 17 may be caused to generate trouble, such as a short circuit or moisture penetration.

The nitride layer 9 (or 19) of the first (or second)

s miconductor device is formed to prot ct the passivation PSG layer 8 (or 18) except for th opening 10 (or 20), so that a side of the layer 8 (or 18) and a portion of the layer 7 (or 17) are exposed in th opening. Therefore, the nitride layer does not sufficiently contribute to improving the moisture-resistance of the semiconductor device.

An object of the present invention is to improve the prevention of moisture penetration into the inside of the semiconductor device.

Another object of the present invention is to provide a semiconductor device avoiding the short circuit caused by damage when blowing a fuse.

The above-mentioned objects and other objects of the present invention are attained by providing a semiconductor device with a fuse comprising: a semiconductor substrate; a field oxide layer formed on the semiconductor substrate; a fuse formed on the field oxide layer; an insulating layer over the fuse and the field oxide layer; a passivation layer formed on the insulating layer and having an opening above the fuse; and a nitride layer formed on the passivation layer; according to the present invention, the semiconductor device further comprises a metal guard ring which surrounds a narrow blowable portion of the fuse, and is formed under the passivation layer to extend to the semiconductor substrate through the insulating layer and the field oxide layer

Preferably, the semiconductor substrate consists of a base semiconductor substrate having a first conductivity and an epitaxial semiconductor layer having a second conductivity, opposite to the first conductivity, and is provided with an isolation region of the first conductivity which region is formed in the epitaxial semiconductor layer so as to completely surround and isolate a portion of the epitaxial layer below the narrow portion, and the metal guard ring that comes into direct contact with the isolation region.

It is possible to form a trench isolation layer of an insulator which extends to the base semiconductor substrate through the epitaxial semiconductor layer to completely surround and isolate a portion of the epitaxial layer below the narrow portion, and the metal guard that is directly formed on the isolation layer.

Preferably, the nitride layer extends on a portion of the insulating layer exposed in the opening except at least a part of which extends above the narrow portion of the fuse.

The present invention will be more apparent from the description of the preferred embodiments set forth below, with reference to the accompanying drawings, in which:

Fig. 1A is a schematic plan view of a first conventional semiconductor d vice of which an insulation layer, a passivation layer and a nitride layer are removed;

Fig. 1B is a schematic sectional view of the first c nventional semiconductor device taken along line B-B of Fig. 1A;

Fig. 2A is a schematic plane view f a s cond conventional semiconductor device of which an insulating layer, a nitride layer and a p rtion of a passivation layer are removed;

Fig. 2B is a schematic sectional view of the second conventional semiconductor device taken along line B-B of Fig. 2A;

Fig. 3A is a schematic plan view of a semiconductor device according to a first embodiment of the present invention of which a passivation layer, a nitride layer and a portion of an insulating layer are removed;

Fig. 3B is a schematic sectional view of the second conventional semiconductor device taken along line B-B of Fig. 3A; and

Fig. 4 is a schematic sectional view of a semiconductor device with a trench isolation layer according to another embodiment of the present invention.

First Embodiment

Referring to Figs. 3A and 3B, a portion of a semiconductor device according to a first embodiment of the present invention including a fuse comprises a semiconductor substrate 31 consisting of a p-type silicon base substrate 32 and an n-type epitaxial silicon layer 33 formed thereon. In the epitaxial layer 33 a p-type isolation region 34 of a rectangular ring (Fig. 3A) is formed by doping acceptor impurities therein to extend in the base substrate 32, so that a portion 33A of the epitaxial layer 33 below a narrow blowable portion 35A of a fuse is isolated from the base substrate 32 and the other portion of the epitaxial layer 33 in a manner similar to that of the first conventional semiconductor device. A field oxide layer 36 of SiO_2 is formed on the epitaxial layer 33 by, e.g., thermally oxidizing the silicon layer 33.

A polycrystalline silicon layer is deposited on the field oxide layer 36 by a chemical vapor deposition (CVD) process and is patterned by lithography to form a fuse 35 having the narrow portion 35A. The field oxide layer 36 is selectively etched by lithography to form a groove surrounding the narrow portion 35A except for two portions under the fuse 35 at the isolation region 34. The groove is separated into the same two portions with a light channel shape. A first metal guard ring 41A of, e.g., aluminum is formed by depositing a metal layer and selectively etching it to overfill the groove only and come into contact with the isolation regi n 34. The first guard ring 41A is separated into the same two portions with a light channel shape, as sh wn in Fig. 3A. It is pr ferable that the f rmati n of the first guard m tal ring 41A is carried out, at the same time (lower) interconn ctions (conductive lin s) are form d. It is possible that the fuse 35 is mad f metal, such as aluminum (Al), tung-

sten (W), tungsten silicide (WSi), titanium (Ti) and titanium nitride (TiN), instead of polycrystalline silicon.

Then, an insulating layer 37 of, e.g., PSG is formed over the metal guard ring 42, the fuse 35 and the field oxide layer 36 by a CVD process and is selectively etched by lithography to form another groove being the same shape as the above-mentioned groove. A second metal guard ring 41B of, e.g., aluminum is formed by depositing a metal layer and selectively etching it to overfill the groove only and come into contact with the first metal ring 41A. The second guard ring 41B is separated into the same two portions with a light channel shape being the same as the first guard ring 41A. It is preferable that the formation of the second guard metal ring 41B is carried out, at the same time other (upper) interconnections (conductive lines) are formed. The second guard ring 41B is jointed to the first guard ring 41A to form a solid metal guard ring 41. Thus, portions of the layers 36 and 37 near the narrow portion 35A are substantially separated from the remaining portions of the layers 36 and 37 with the metal guard ring 41. It is preferable that one of the metal guard rings 41A and 41B is connected with an interconnection (conductive line) for applying a bias voltage to the isolating region 34. It is possible to use aluminum alloy W, WSi, Ti or TiN, as a conductive material of the metal guard ring.

A passivation layer 38 of, e.g., PSG is formed over the metal guard ring 41 and the insulating layer 37, and is selectively etched to form an opening 40 above the narrow portion 35A. Then, a nitride layer 39 of, e.g., Si_3N_4 is formed on the passivation layer 38 and within the opening 40 to cover the exposed side of the layer 38 and the exposed portion of the layer 37. The nitride layer 39 is selectively etched to form another opening 42 above the narrow portion 35A in the opening 40, as shown in Fig. 3A. The opening 42 is smaller than the opening 40, so that the nitride layer 39 covers the side of the passivation layer 38 and an interface between the layers 37 and 38, but does not exist above the narrow portion 35A. Thus, the semiconductor device with the fuse is obtained.

The fuse 15 of the semiconductor device is blown by breaking the narrow portion 15A with a laser beam or a pulse current in the conventional manner. Some of a number of the fuses are selectively blown in accordance with demands, while the majority of the fuses are not blown.

According to the present invention, the metal guard ring 42 vertically extends through the layer 36 and 37 and comes into contact with the substrate 31 (epitaxial layer 33), which prevents moisture from pen trating int th inside f the d vic through the insulating (hygrosc picity) layer 37, and through cracks caus d during blowing and int rfaces between the layers 37 and 36 and between the layer 36 and the substrate 31. The nitride layer 39 covers the side of the passivation layer 38 and the interface b tween the layers 38 and 37 as well as the top surface of the layer 38 to prevent moisture from penetrating through the layer 38 and the interface. Furthermore, the isolation region 34 prevents the short circuit trouble as mentioned in the prior art explanation. Since the metal guard rind 41 comes into contact with the isolation region, when an bias voltage is applied to the isolation region 34 through the metal guard ring 41, an electrical isolation effect of the isolation region is increased. For example, the lowest voltage is applied to the p-type isolation region 34 through the metal guard ring 41 to intensify the isolation effect, which more certainly prevents the short circuit trouble.

Second Embodiment

Referring to Fig. 4, a semiconductor device according to a second embodiment of the present invention is similar to the device of the first embodiment except that a trench isolation layer 45 is formed in the substrate instead of the isolation region. Preferably, the trench isolation layer 45 comprises a thin SiO_2 layer 46 formed on a U-groove, a filler 47 of, e.g., polycrystalline silicon and a lid SiO_2 layer 48 of the filler. Reference numerals in Fig. 4 which are the same as those used in Figs. 3A and 3B indicate the same parts or similar parts of the device of Figs. 3A and 3B.

After the growth of the epitaxial layer 33 of the substrate 31, the substrate 31 is selectively and anisotropically etched by, e.g., a reactive ion etching (RIE) process to form a U-groove of a rectangular ring similar to the isolation region 34 (Fig. 3A). The groove extends in a semiconductor base substrate 32. The substrate 31 is thermally oxidized to form the thin SiO_2 layer 46 on the groove surface and at the same time a thin SiO_2 layer (not shown) on the top surface of the epitaxial layer 33. A polycrystalline silicon is deposited over the whole surface to fill the groove and is then removed to leave a portion thereof within the groove as the filler 47. The thin SiO_2 layer formed on the epitaxial layer 33 is removed by an etching process. Next, an upper portion of the filler 47 and the epitaxial layer 33 are thermally oxidized to form the lid SiO_2 layer 48 and the field oxide layer 36. Thus, the trench isolation layer 45 is formed.

As mentioned in the first embodiment, the fuse with the narrow blowable portion 35A, the first metal guard ring 41A coming into contact with the lid SiO_2 layer 48, the insulating layer 37, the second metal guard ring 41B, the passivation layer 38 with the opening 40, and the nitride lay r 39 with the opening 42 are formed to produce the semiconductor device.

Th metal guard ring 41 consisting of the first and second m tal guard ring 41A and 41B and the nitride layer 39 extending in the groove 40 prevent moisture from penetrating in the inside of the device. The trench isolation layer 45 prevents the short circuit

troubl . Therefore, quality of the semiconductor device with a fuse is remarkable improved.

Claims

1. A semiconductor device with a fuse comprising:
   a semiconductor substrate (31);
   a field oxide layer (36) formed on said semiconductor substrate;
   a fuse (35) formed on said field oxide layer (36);
   an insulating layer (37) over said fuse (35) and said field oxide layer (36);
   a passivation layer (38) formed on said insulating layer and having an opening above said fuse (35); and
   a nitride layer (39) formed on said passivation layer (38); characterized in that said semiconductor device further comprises a metal guard ring (41) which surrounds a narrow blowable portion (35A) of said fuse (35), and is formed under said passivation layer (38) to extend to said semiconductor substrate (31) through said insulating layer (37) and said field oxide layer (36).

2. A semiconductor device according to claim 1, wherein said semiconductor substrate (31) consists of a base semiconductor substrate (32) having a first conductivity and an epitaxial semiconductor layer (33) having a second conductivity, opposite to said first conductivity, and is provided with an isolation region (34) of said first conductivity which region is formed in said epitaxial semiconductor layer (33) so as to completely surround and isolate a portion (33A) of said epitaxial layer below said narrow portion (35A), and said metal guard comes into direct contact with said isolation region (34).

3. A semiconductor device according to claim 1, wherein said semiconductor substrate (31) consists of a base semiconductor substrate (32) having a first conductivity and an epitaxial semiconductor layer (33) having a second conductivity, opposite to said first conductivity, and is provided with a trench isolation layer (45) of an insulator which extends to said base semiconductor substrate (32) through said epitaxial semiconductor layer (33) so as to completely surround and isolate a portion (33A) of said epitaxial layer below said narrow portion (35A), and said metal guard comes into direct contact with said isolation layer.

4. A semiconductor device according to any one of the preceding claims, wherein said nitride layer (39) extends on a portion of said insulating layer (37) expos d in said opening (40) except at least a part thereof extending above the narrow p rtion (35A) of said fuse.

5. A semiconductor device acc rding to any one of the preceding claims, wherein said fuse (35) is made of polycrystalline silicon, aluminum, tungsten, tungsten silicide, titanium or titanium nitride.

6. A semiconductor device according to any one of the preceding claims, wherein said metal guard ring (41) is made of aluminium, aluminium alloy or polycrystalline silicon.

7. A semiconductor device according to any one of the preceding claims, wherein said insulating layer (37) is made of SiO_2 and said passivation layer (38) is made of PSG.

Fig. 1A

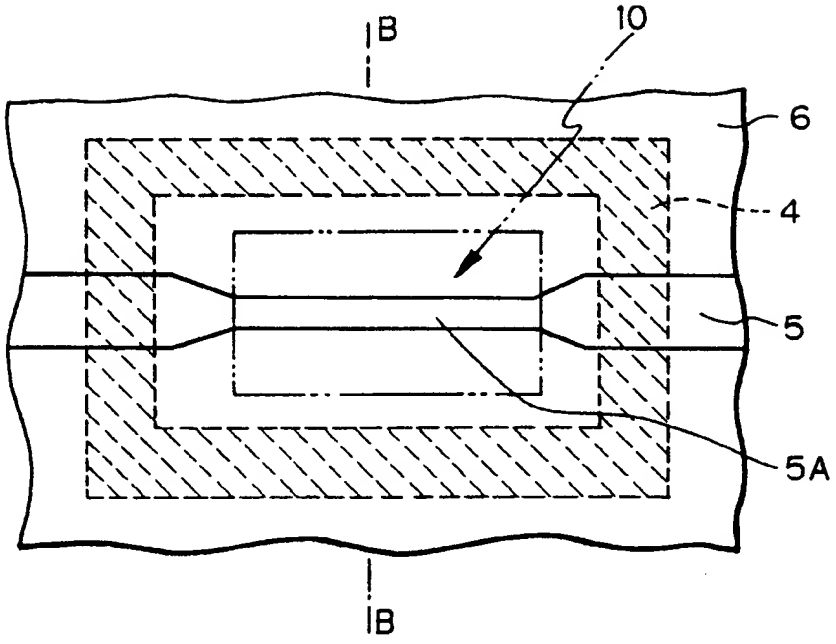


Fig. 1B

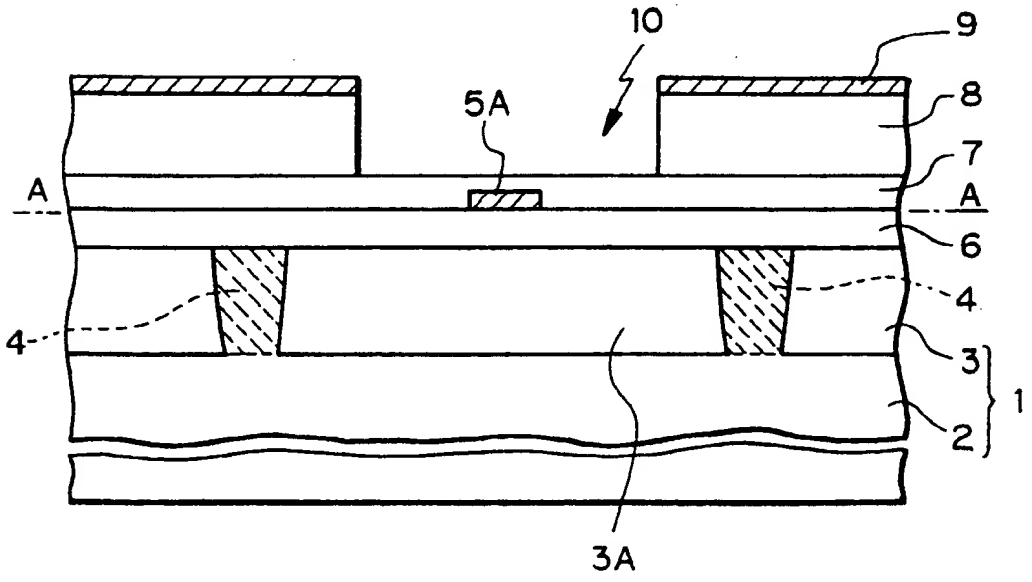


Fig. 2A

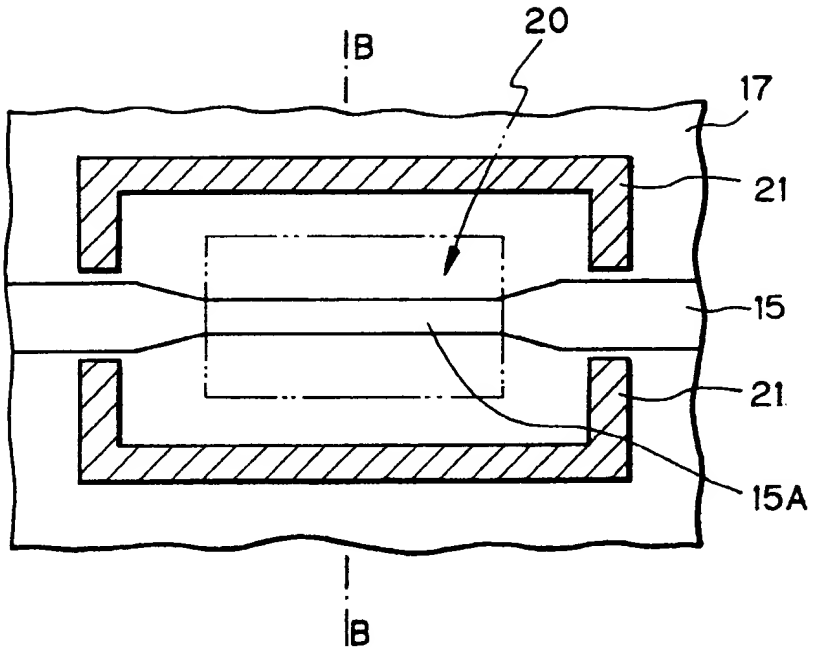


Fig. 2B

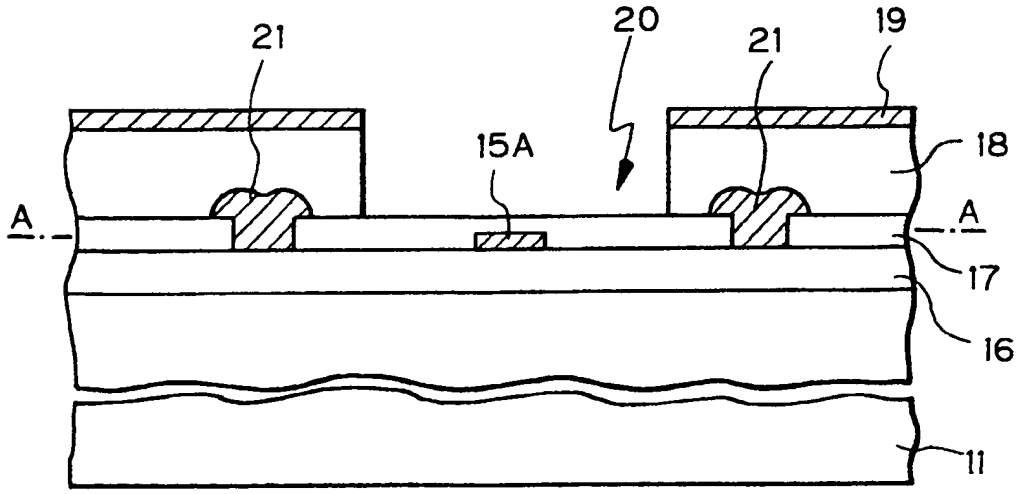


Fig. 3A

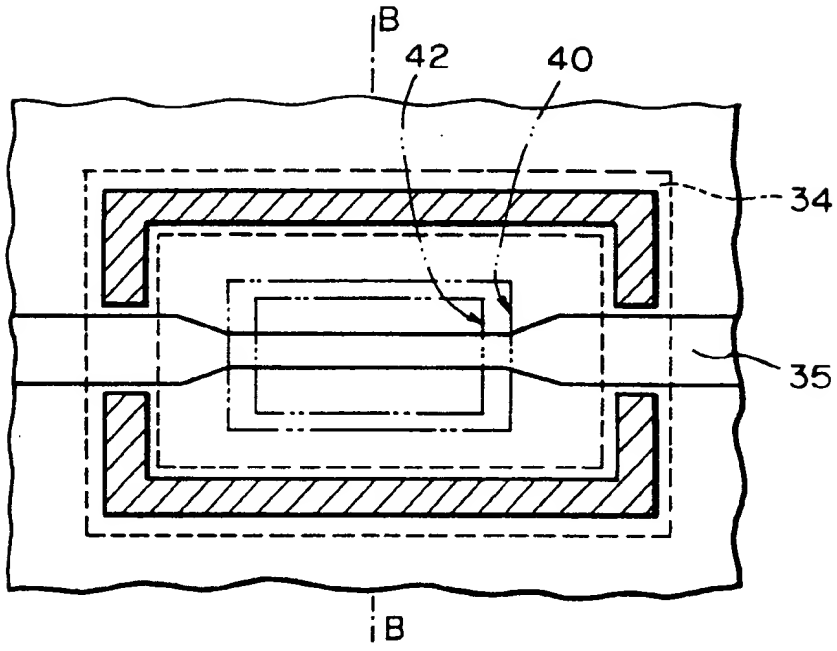


Fig. 3B

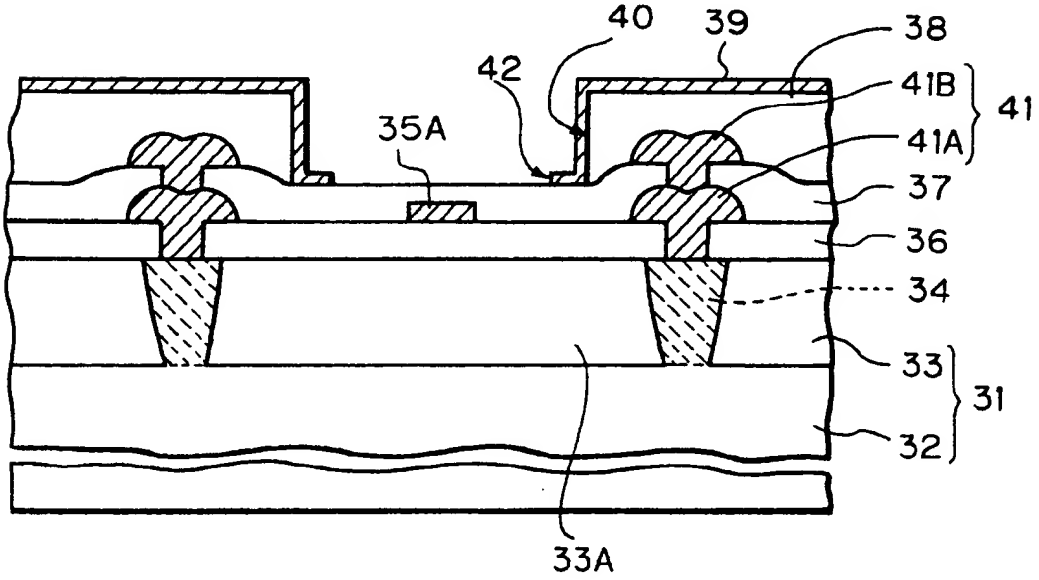
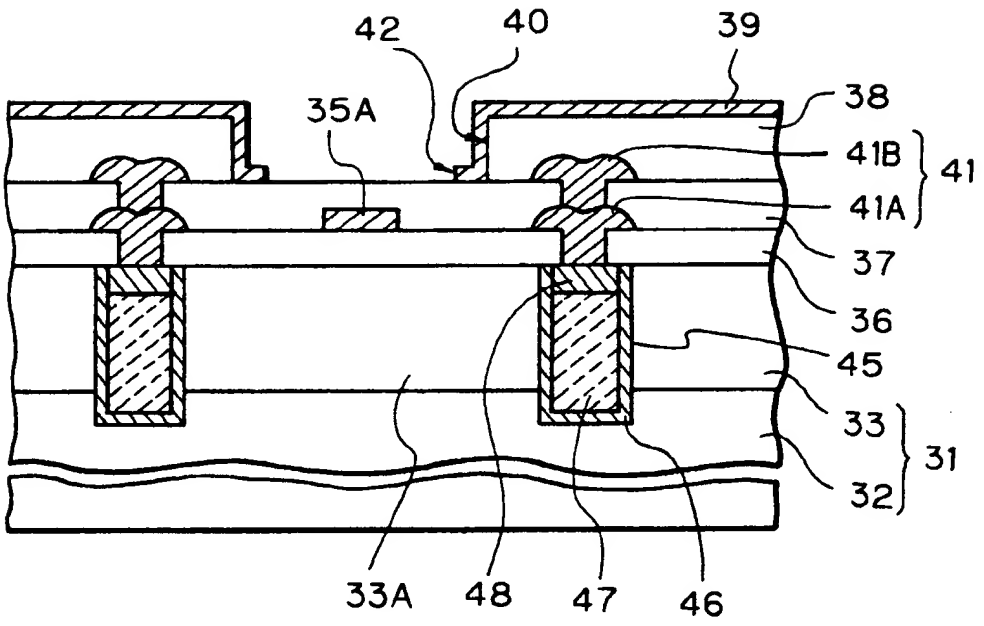


Fig. 4



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EUROPEAN SEARCH REPORT

Application Number
EP 92 30 7992

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	PATENT ABSTRACTS OF JAPAN vol. 9, no. 248 (E-347)4 October 1985 & JP-A-60 098 664 (MITSUBISHI) 1 June 1985 * abstract *	1	H01L23/525
A		6	
Y	EP-A-0 025 347 (FUJITSU) * page 2, line 16 - line 23; claims 1,4,6; figure 4 *	1	
A		4,5,7	
A	EP-A-0 241 046 (NEC) * claims 1,3,6; figure 5 *	1-3,5	
A	EP-A-0 112 693 (FUJITSU)		
A	EP-A-0 076 967 (TOSHIBA)		

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 DECEMBER 1992	DE RAEVE R.A.L.

CATEGORY OF CITED DOCUMENTS

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